OPTIMIZED CONTAINER STACKED CAPACITOR DRAM CELL UTILIZING SACRIFICIAL OXIDE DEPOSITION AND CHEMICAL MECHANICAL POLISHING

CROSS-REFERENCE TO RELATED APPLICATION

This is a continuation to U.S. patent application Ser. No. 07/850,746, filed Mar. 13, 1992, now U.S. Pat. No. 5,162,248.

FIELD OF THE INVENTION

This invention relates to semiconductor circuit memory storage devices and more particularly to a process for fabricating three-dimensional stacked capacitor structures that may be used in such storage devices as high-density dynamic random access memories (DRAMs).

BACKGROUND OF THE INVENTION

In dynamic semiconductor memory storage devices it is essential that storage node capacitor cell plates be large enough to retain an adequate charge or capacitance in spite of parasitic capacitances and noise that may be present during circuit operation. As is the case for most semiconductor integrated circuitry, circuit density is continuing to increase at a fairly constant rate. The issue of maintaining storage node capacitance is particularly important as the density of DRAM arrays continues to increase for future generations of memory devices.

The ability to densely pack storage cells while maintaining required capacitance levels is a crucial requirement of semiconductor manufacturing technologies if future generations of expanded memory array devices are to be successfully manufactured.

One method of maintaining, as well as increasing, storage node size in densely packed memory devices is through the use of "stacked storage cell" design. With this technology, two or more layers of a conductive material such as polycrystalline silicon (polysilicon or poly) are deposited over an access device on a silicon wafer, with dielectric layers sandwiched between each poly layer. A cell constructed in this manner is known as a stacked capacitor cell (STC). Such a cell utilizes the space over the access device for capacitor plates, has a low soft error rate (SER) and may be used in conjunction with inter-plate insulative layers having a high dielectric constant.

However, it is difficult to obtain sufficient storage capacitance with a conventional STC capacitor as the storage electrode area is confined within the limits of its own cell area. Also, maintaining good dielectric breakdown characteristics between poly layers in the STC capacitor becomes a major concern once insulator thickness is appropriately scaled.

A paper submitted by N. Shinmura, et al., entitled "A Stacked Capacitor Cell with Ring Structure," Extended Abstracts of the 22nd International Conference on Solid State Devices and Materials, 1990, pp. 833–836, discusses a 3-dimensional stacked capacitor incorporating a ring structure around the main electrode to effectively double the capacitance of a conventional stacked capacitor.

The ring structure and its development is shown in FIGS. 1(*c*) through 1(*g*), pp. 834 of the article mentioned above. FIG. 1(*a*), on the same page shows a bird's eye-view of storage electrodes. The storage node is formed by two polysilicon layers that form a core electrode encircled by a ring structure. Capacitor dielectric film surrounds the whole surface of the storage node electrode and then is covered with a third polysilicon layer to form the top capacitor electrode and completes the storage cell. This design can be fabricated using current methods and increases storage capacitance by as much as 200%.

Also, in a paper submitted by T. Kaga, et al., entitled "Crown-Shaped Stacked-Capacitor Cell for 1.5-V Operation 64-Mb DRAM's," IEEE Transactions on Electron Devices. VOL. 38, NO. 2, February 1991, pp. 255–261, discusses a self-aligned stacked-capacitor cell for 64-Mb DRAM's, called a CROWN cell. The CROWN cell and its development are shown in FIGS. 7(*d*) through 7(*f*), pp. 258 of this article. The crown shaped storage electrode is formed over word and bit lines and separated by a oxide/nitride insulating layer with the top insulating layer being removed to form the crown shape. Capacitor dielectric film surrounds the whole surface of the storage node electrode and the top capacitor electrode is formed to complete the storage cell.

The present invention develops an existing stacked capacitor fabrication process to construct and optimize a three-dimensional container stacked capacitor cell. The capacitor's bottom plate (or storage node plate) is centered over a buried contact (or node contact) connected to an access transistor's diffusion area. The method presented herein provides fabrication uniformity and repeatability of the three-dimensional container cell.

SUMMARY OF THE INVENTION

The invention is directed to maximizing storage cell surface area in a high density/high volume DRAM (dynamic random access memory) fabrication process. An existing capacitor fabrication process is modified to construct a three-dimensional stacked container capacitor. The capacitor design of the present invention defines a stacked capacitor storage cell that is used in a DRAM process, however it will be evident to one skilled in the art to incorporate these steps into other processes requiring volatile memory cells, such as VRAMs or the like.

After a silicon wafer is prepared using conventional process steps, the present invention develops the container capacitor by etching a contact opening into a low etch rate oxide. The contact opening is used as a form for deposited polysilicon that conforms to the sides of the opening walls. Within the thin poly lining of the oxide container a high etch-rate oxide, such as ozone TEOS, is deposited over the entire structure thereby bridging across the top of the oxide container. The high etch-rate oxide is planarized back to the thin poly by using Chemical Mechanical Polishing (CMP). This CMP step is selective such that oxide is removed with sufficient overetch and stops on the thin poly. The resulting exposed poly is then removed to separate neighboring containers either through an isotropic wet poly etch or an additional CMP with the chemical aspect modified to now etch and selectively remove the poly and not the oxide. The two oxides, having different etch rates, are then etched by a single wet dilute BOE etch step, thereby leaving a free-standing poly container cell, with all the inside (high etch rate) oxide removed, that

is equal in height to the depth of the original contact opening. In addition, a pre-determined amount of low etch rate oxide is removed thereby leaving oxide surrounding the container, poly for both structural support and process integration for further processing which requires oxide to be left above the word lines.

The present invention uses a higher etch-rate oxide inside the container to block the container poly etch. This high etch rate oxide is completely removed during oxide etch back. This protects the container during processing without adding photoresist and introducing extra processing steps or unwarranted contaminants. A standard CMP oxide etch is utilized that allows fabrication uniformity and repeatability across the wafer which cannot be achieved by resist filled container processes.

Another advantage of filling the container with high etch rate oxide is that the poly can be etched with a low cost, timed wet poly etch, while partially filled containers (as seen in FIG. 9), due to inherent recession of resist 92 height (to allow for sufficient process margin), will not allow a wet poly etch without loss in cell height 93, loss in uniformity and repeatability across the wafer's surface. Because this invention can be etched isotropically at poly etch, it avoids the recessing (overetch of the storage poly container 93 in FIG. 9) and splintering effects caused by a dry etch poly process.

As seen in FIG. 10, splintering effects 101 of storage node poly 93 result from a dry anisotropic etch (due to non-uniform etching of polycrystalline silicon 93) because the plasma etch reacts faster along heavily doped grain boundaries. Splinters 101 later tend to 'break off' in subsequent processing leading to contamination particulates. The trenching of the poly leads to the sidewalls of the poly container to be exposed, thus making it impossible to wet etch the oxide around the cell without translating the trenched poly horizontal portion of the etch into surrounding oxide 91 thereby leaving a ring of thin oxide around he container cell.

The present invention also protects the vertical sidewall of the oxide form by covering it with poly, thereby making a horizontal wet oxide etch back possible. In addition, all films which see etch processing, CMP or otherwise, are subsequently removed thereby acting as sacrificial films such that particles created during the CMP etch do not contaminate the inside of the poly container.

FIG. 1 shows a gray scale reproduction of a SEM photograph of an array of poly containers 12 which demonstrates the uniformity and repeatability of poly containers 12 across substrate that results from utilizing the process steps of the present invention discussed hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a gray-scale reproduction of a SEM (Scanning Electronic Microscope) photograph of a cross-sectional view of an array of container poly rings;

FIG. 2 is a composite cross-sectional view of an in-process wafer portion depicting the beginning steps of the present invention, said steps comprising forming a planarized layer of low etch rate oxide, etching a buried contact and placing a thin layer of conformal poly;

FIG. 3 is a cross-sectional view of the in-process wafer portion of FIG. 2 after formation of a layer of high etch rate oxide;

FIG. 4 is a cross-sectional view of the in-process wafer portion of FIG. 3 after planarization of the high etch rate oxide;

FIG. 5 is a cross-sectional view of the in-process wafer portion of FIG. 4 following a wet etch back of the exposed thin poly layer;

FIG. 6 is a cross-sectional view of the in-process wafer portion of FIG. 5 following an etch of both low etch rate and high etch rate oxides;

FIG. 7 is a cross-sectional view of the in-process wafer portion FIG. 6 following blanket formations of conformal cell dielectric and polysilicon, respectively;

FIG. 8 is a cross-sectional view of a storage cell created by the present invention when integrated into a stacked capacitor fabrication process; and

FIG. 9 is a composite cross-sectional view of an in-process wafer portion depicting a container cell filled with photoresist prior to patterning; and

FIG. 10 is a composite cross-sectional view of the in-process wafer portion of FIG. 9 depicting splintering of storage node poly and formation of a thin ring of oxide surrounding the storage node poly following an anisotropic etching to pattern a container cell.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The invention is directed to maximizing storage cell surface area, as well as providing uniform and repeatable, defect free, storage cell structures across a given substrate, in a high density/high volume DRAM fabrication process, in a sequence shown in FIGS. 2–7.

A silicon wafer is prepared using conventional process steps up to the point of processing an array of storage cell capacitors. Capacitor cell fabrication will now follow.

The storage capacitor of each memory cell will make contact directly to an underlying diffusion area. Each underlying diffusion area will have two storage node connections isolated from a single digit line contact by access transistors formed by poly word lines crossing the active area. Normally each diffusion area within the array is isolated from one another by a thick field oxide. The diffusion areas can be arranged in interdigitated columns and non-interdigitated rows or simply parallel and in line to one another in both the vertical and horizontal directions. As previously mentioned, the diffusion areas are used to form active MOS transistors (serving as access transistors to each individual capacitor) that can be doped as NMOS or PMOS type FETs depending on the desired use.

Referring now to FIG. 2, a thick layer of low etch rate oxide 21 is formed over an existing topography of a given substrate. Oxide 21 is then planarized, preferably by chemical-mechanical planarization (CMP) techniques down to a predetermined thickness. The thickness of planarized oxide 21 depends on the height that is desired for the poly container structure yet to be formed. The height of the resulting poly structure will determine the capacitor plate surface area that will be required to sufficiently hold a charge. It has been shown that a structure of approximately 1.0–1.5μ is sufficient to construct a reliable 64M DRAM cell using optimized cell dielectric (Container height depends on such factors as container diameter, dielectric constant and thickness of oxides used which are brought to light in the continuing discussion.). A contact opening 22 is then etched into oxide 21 thereby allowing access to the underlying topography (for DRAM capacitor purposes